

CLAIMS

What is claimed is:

- 1 1. An RF power amplifier formed using an integrated circuit, comprising:
2 a power amplifier circuit; and
3 a serial interface formed using the integrated circuit for sending and receiving signals.
- 1 2. The RF power amplifier of claim 1, wherein the integrated circuit includes a
2 plurality of pins, the RF power amplifier further comprising:
3 a mode control pin for selecting a first mode or a second mode; and
4 a first interface pin, wherein the first interface pin has a first function in the first mode
5 and a second function in the second mode.
- 1 3. The RF power amplifier of claim 2, further comprising a second interface pin,
2 wherein the second interface pin has a first function in the first mode and a second
3 function in the second mode.
- 1 4. The RF power amplifier of claim 2, wherein the first mode is a serial interface
2 mode and the second mode is a pin control mode.
- 1 5. The RF power amplifier of claim 2, wherein the mode control pin is used as an
2 internal voltage source in the power amplifier.

1 6. The RF power amplifier of claim 5, wherein the mode control pin is used as an
2 internal voltage source in the power amplifier only when the first mode is selected.

1 7. The RF power amplifier of claim 1, wherein the RF power amplifier further
2 comprises:
3 a plurality of pins for coupling to a serial bus; and
4 a low pass filter coupled to one of the pins for filtering control signals to reduce RF noise.

1 8. The RF power amplifier of claim 1, wherein the RF power amplifier further
2 comprises:
3 a plurality of pins for coupling to a serial bus; and
4 a gate circuit coupled to a first pin for selectively blocking the signal received at the first
5 pin.

1 9. The RF power amplifier of claim 8, wherein the signal is blocked when the RF
2 power amplifier is enabled.

1 10. The RF power amplifier of claim 8, wherein the first pin receives a serial clock
2 signal.

1 11. The RF power amplifier of claim 1, wherein the RF power amplifier further
2 comprises:
3 a serial data output pin for coupling to a serial bus; and

4 a tri-state driver coupled to the serial data output pin.

1 12. The RF power amplifier of claim 11, wherein the tri-state driver tri-states the
2 output pin while the RF power amplifier is transmitting.

1 13. The RF power amplifier of claim 12, further comprising a bias circuit for biasing
2 the tri-stated output pin while the RF power amplifier is transmitting.

1 14. A wireless communication device comprising:
2 a controller circuit adapted to control the operation of the communication device;
3 a transceiver;
4 an RF power amplifier; and
5 a serial bus coupled to the controller, transceiver, and RF power amplifier.

1 15. The wireless communication device of claim 14, wherein the power amplifier
2 includes a sensor for sensing a property of the power amplifier.

1 16. The wireless communication device of claim 15, wherein information from the
2 sensor is transmitted to the controller over the serial bus.

1 17. The wireless communication device of claim 16, wherein the sensor is a
2 temperature sensor.

1 18. The wireless communication device of claim 14, wherein the controller transmits
2 a band control signal to the transceiver over the serial bus, and wherein the power

3 amplifier monitors the serial bus and automatically selects a band based on the band
4 control signal.

1 19. The wireless communication device of claim 14, wherein the serial bus is disabled
2 when the power amplifier is enabled.

1 20. The wireless communication device of claim 14, wherein the power amplifier
2 includes a mode control pin which selects a serial interface mode or a pin control mode.

1 21. The wireless communication device of claim 20, further comprising a coupling
2 between the controller and the mode control pin, wherein the controller supplies the
3 power amplifier with a voltage supply via the connection to the mode control pin.

1 22. The wireless communication device of claim 14, wherein the serial bus is disabled
2 when the power amplifier is transmitting.

1 23. The wireless communication device of claim 14, wherein the power amplifier
2 further comprises:
3 a plurality of pins for coupling to a serial bus; and
4 a low pass filter coupled to one of the pins for filtering control signals to reduce RF noise.

1 24. The wireless communication device of claim 14, wherein the power amplifier
2 further comprises:
3 a plurality of pins for coupling to a serial bus; and

4 a gate circuit coupled to a first pin for selectively blocking the signal received at the pin.

1 25. The wireless communication device of claim 24, wherein the signal is blocked
2 when the power amplifier is enabled.

1 26. The wireless communication device of claim 25, wherein the first pin receives a
2 serial clock signal.

1 27. The wireless communication device of claim 14, wherein the power amplifier
2 further comprises:
3 a serial data output pin for coupling to a serial bus; and
4 a tri-state driver coupled to the serial data output pin.

1 28. The wireless communication device of claim 27, wherein the tri-state driver tri-
2 states the output pin while the power amplifier is transmitting.

1 29. The wireless communication device of claim 28, further comprising a bias circuit
2 for biasing the tri-stated output pin while the power amplifier is transmitting.

1 30. A method of controlling an RF power amplifier in a wireless communications
2 device, comprising:
3 providing a baseband controller connected to a digital bus;
4 providing an RF power amplifier having a serial interface for communicating with the
5 digital bus; and

6 coupling the serial interface of the RF power amplifier to the digital bus.

1 31. The method of claim 30, wherein the power amplifier transmits signals in periodic
2 bursts, and wherein the digital bus is disabled during the bursts.

1 32. The method of claim 30, wherein the serial interface of the power amplifier uses a
2 plurality of pins, the method further comprising the step of coupling a low pass filter to at
3 least one of the pins.

1 33. The method of claim 30, wherein the serial interface of the power amplifier uses a
2 plurality of pins, the method further comprising the step of blocking the signal provided
3 to a first pin of the power amplifier serial interface when the power amplifier is
4 transmitting.

1 34. The method of claim 30, further comprising providing a serial data output pin at
2 the serial interface of the power amplifier; and when the power amplifier is transmitting,
3 biasing the serial data output pin.

1 35. The method of claim 30, further comprising providing a serial data output pin at
2 the serial interface of the power amplifier; and when the power amplifier is transmitting,
3 tri-stating the serial data output pin.

1 36. The method of claim 35, further comprising biasing the tri-stated output pin.

1 37. The method of claim 30, further comprising sensing a condition in the power
2 amplifier; and sending information relating to the sensed condition over the digital bus.

1 38. The method of claim 37, wherein the sensed condition is temperature.

1 39. The method of claim 37, further comprising shutting down the RF power
2 amplifier in response to the sensed condition.

1 40. The method of claim 39, the RF power amplifier is shut down when a threshold
2 temperature is sensed.